A Novel Technique For Fast Multiplication

Sait, S.M. Farooqui, A.A. Beckhoff, G.F.;King Fahd Univ. of Pet.Miner., Dhahran;
Computers and Communications, 1995. Conference Proceedings of the 1995 IEEE Fourteenth Annual International Phoenix conference;Publication Date: 28-31 Mar 1995;ISBN: 0-7803-2492-7
King Fahd University of Petroleum & Minerals

http://www.kfupm.edu.sa

Summary

In this paper we present the design of a new high speed multiplication unit. The design is based on non-overlapped scanning of 3-bit fields of the multiplier. In this algorithm the partial products of the multiplicand and three bits of the multiplier are pre-calculated using only hardwired shifts. These partial products are then added using a tree of carry-save-adders, and finally the sum and carry vectors are added using a carry-look-ahead adder. In case of 2's complement multiplication the tree of carry-save-adders also receives a correction output produced in parallel with the partial products. The algorithms is modeled in a hardware description language and its VLSI chip implemented. The performance of the new design is compared with other recent ones proposed in literature